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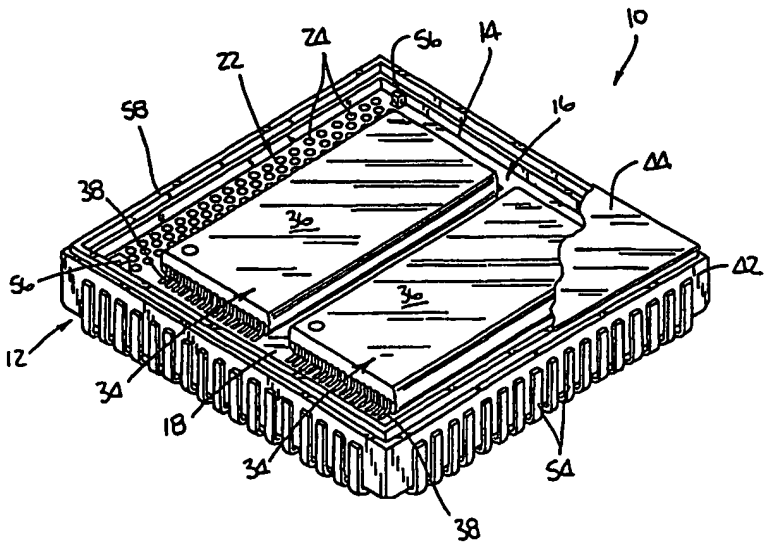

(57) Abstract

A chip module (10) comprising a chip array (14) which includes an interconnect substrate (16) having opposed, generally planar surfaces and a first interconnect pad array (22) disposed on at least one of the surfaces. Attached to the interconnect substrate (16) is at least one integrated circuit chip (34) which is electrically connected to the first interconnect pad array (22). Chip module (10) further comprises a package (12) which comprises a main body (42) defining a cavity sized and configured to receive chip array (14) and having a generally planar interconnect shelf which extends within the cavity and includes a second interconnect pad array disposed thereon. The package (12) also includes a lid (44) attachable to main body (42). The chip array (14) is insertable into the cavity such that the first and second interconnect pad arrays are in aligned contact with each other and the attachment of lid (44) to main body (42) encloses and seals the chip array (14) within package (12).

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UNIVERSAL PACKAGE AND METHOD OF FORMING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS
(Not Applicable)

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT
(Not Applicable)

BACKGROUND OF THE INVENTION

The present invention relates generally to chip modules, and more particularly to a chip module including a highly configurable chip array which is interconnectable to a universal package capable of hermetically sealing the chip array.

There is currently known in the prior art chip modules comprising a chip array which is mounted into a package for purposes of protecting the chip array from contaminants such as dust and moisture. The package may also be used to convert the chip array to a particular standard pin format. The chip array typically comprises a substrate (e.g., a circuit board) having off-the-shelf, pre-packaged memory or logic devices (e.g., TSOP packaged chips) mounted to one or both of the opposed sides or faces thereof. This chip array is mounted into and sealed within the associated package of the chip module. These prior art chip modules wherein the chip array is sealed within the package to protect the same from contaminants are often used to achieve compliance with stringent military standards such as the JET "X" standard which require extremely low susceptibility to component failure as a result of contamination from external or environmental sources.

Though prior art chip modules are generally suitable for protecting the chip array within the associated package from external contamination, they possess numerous deficiencies which detract from their overall utility. One such deficiency lies in the inability to

test the currently known chip modules until the completion of the package assembly process. Due to the complexity of their construction which is attributable in large part to the heat and moisture sensitivity of the internal chip array, such chip modules experience a relatively high failure rate during initial testing. Another deficiency lies in the inability to recover components from these chip modules in the event the same are unsuccessfully tested. For example, if the failure of the chip module during testing is attributable to a soldering problem, the chip module must be scrapped in its entirety due to the currently known configurations and assembly methods related thereto not allowing for the recovery or salvage of either the chip array or the package.

A further deficiency of the prior art chip modules is that the package thereof is device specific, i.e., tailored to accommodate a particular chip array. As such, since the chip array is not confined to one specific configuration but may have any one of a multitude of differing configurations, any particular chip array will typically require a different device specific package. In this respect, the development of a new chip array carries with it the need to develop a new package, and hence new tooling as well as a new assembly protocol. As will be recognized, these constantly changing tooling and assembly requirements significantly increase the product costs of prior art chip modules. Moreover, the configuration of such prior art chip modules, and in particular the chip arrays thereof, does not lend itself to use with newly developed memory or logic devices, thus increasing susceptibility to obsolescence.

The present invention addresses and overcomes these deficiencies of prior art chip modules by providing a low cost, high reliability, high density chip module wherein a highly configurable, custom chip array is

interconnectable to a "universal" package. In the present chip module, the chip array includes a novel and unique interconnect substrate having an interconnect array which is specifically adapted to electrically communicate with a corresponding interconnect array provided within a cavity of the package. In view of the complementary nature of these interconnect arrays, the package is universal in the sense that it may be used in conjunction with any chip array including the interconnect substrate. The package in the present chip module, in addition to being usable with any chip array including the interconnect substrate, is adapted to convert such chip array to a standard sixty-eight (68) pin format.

In addition to providing economies in the manufacturing/assembly process and thereby significantly reducing product cost, the configuration of the present chip module and assembly methodology preferably employed in relation thereto allows for the testing of the chip array prior to the mounting of the same within the package, and the testing of the combined chip array/package prior to the chip array being sealed within the package. As a result, in the present chip module, either the chip array or the package may usually be salvaged in the event of an unsuccessful result being obtained during the testing process. Moreover, the configuration of the chip array of the present chip module provides a high level of adaptability to new memory or logic devices, thus substantially eliminating its susceptibility to rapid obsolescence. The completed chip module formed in accordance with the present invention also satisfies the most stringent military standards. These, and other advantages attributable to the present invention, will be described in more detail below.

BRIEF SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a chip module which includes a universal package for accommodating any one of uniquely configured chip arrays (e.g., memory or logic arrays). In the preferred embodiment, the chip array, which is a sub-assembly of the chip module, comprises an interconnect substrate having opposed, generally planar surfaces and including a first interconnect pad array disposed on at least one of the surfaces thereof. The interconnect substrate preferably has a generally square configuration defining four peripheral edge segments, with the first interconnect pad array extending along one of the peripheral edge segments. The first interconnect pad array itself preferably comprises first and second sets of conductive interconnect pads which are disposed on respective ones of the opposed surfaces of the interconnect substrate and extend along a common peripheral edge segment thereof. The conductive interconnect pads of the first and second sets are arranged in identical patterns such that the conductive interconnect pads of the first set are aligned with respective ones of the conductive interconnect pads of the second set. Additionally, a plurality of vias are preferably extended through the interconnect substrate between respective pairs of the conductive interconnect pads of the first and second sets thus establishing electrical contact or communication between the pads of each pair.

In addition to the interconnect substrate, the chip array of the present chip module comprises at least one integrated circuit chip which is attached to the interconnect substrate and electrically connected to the first interconnect pad array. In the present chip module, the integrated circuit chip is preferably incorporated into a packaged chip having a plurality of chip leads protruding therefrom. The chip leads are

electrically connected to respective ones of a plurality of conductive lead pads which are disposed on at least one of the opposed surfaces of the interconnect substrate and are electrically connected to the first interconnect pad array. It is contemplated that the interconnect substrate of the chip array may include a plurality of conductive lead pads disposed on respective ones of the opposed surfaces thereof, with the chip leads of at least two packaged chips being electrically connected to the conductive lead pads on respective ones of the opposed surfaces of the interconnect substrate. As indicated above, the chip array may comprise a memory array or a logic array, with each of the packaged chips preferably being a memory or logic device selected from the group consisting of a TSOP I package, a TSOP II package, a QFP package, and a CSP package or the like.

Though the interconnect substrate of the chip array of the present chip module may be of a rigid construction, the same is preferably flexible and formed to have a thickness not exceeding about 0.015 inches. Importantly, this minimal thickness of the interconnect substrate, which results in its flexibility, provides the assembled chip array with a thin profile as well. The interconnect substrate is preferably fabricated from a polyamide, though alternative materials possessing similar characteristics may also be employed in relation thereto. Additionally, the interconnect substrate is preferably formed to include a pair of registry notches disposed within respective ones of the peripheral edge segments thereof which extend in generally perpendicular relation to the peripheral edge segment along which the first and second sets of conductive interconnect pads of the first interconnect pad array are extended.

In addition to the chip array, the chip module of the present invention comprises a package including a generally square main body and a lid attachable to the main body. The main body itself defines a cavity sized

and configured to receive the chip array, and has a generally planar interconnect shelf which extends within the cavity and includes a second interconnect pad array disposed thereon. The second interconnect pad array comprises a third set of conductive interconnect pads which are arranged upon the shelf in a pattern identical to those of the first and second sets of conductive interconnect pads of the first interconnect pad array of the chip array. In the preferred chip module, a total of seventy-one (71) conductive interconnect pads are included in each of the first, second and third sets thereof. The main body of the package also includes a plurality of package leads which protrude therefrom and are electrically connected to the second interconnect pad array. More particularly, the main body preferably includes sixty-eight (68) package leads which extend about the periphery thereof. The package (i.e., the main body and lid) is preferably fabricated from co-fired alumina, though alternative materials possessing similar characteristics may also be employed in relation thereto.

In the present chip module, the chip array is insertable into the cavity of the main body such that the first and second interconnect pad arrays are in aligned contact with each other. Subsequent to the insertion of the chip array into the cavity and the electrical connection of the first and second interconnect pad arrays to each other in a prescribed manner, the attachment of the lid to the main body encloses and seals the chip array within the package. In the present chip module, the main body of the package is preferably formed to include an opposed pair of tabs which are insertable into respective ones of the registry notches of the interconnect substrate when the chip array is inserted into the cavity. Advantageously, the receipt of the tabs into the notches facilitates a proper registry between the first and second interconnect pad arrays.

Further in accordance with the present invention, there is provided a method of assembling a chip module. The preferred method comprises the initial step of assembling a chip array of the chip module. Such assembly is accomplished by attaching at least one integrated circuit chip, and more particularly at least two packaged chips, to respective ones of the opposed surfaces of the interconnect substrate such that the packaged chips are electrically connected to the first interconnect pad array of the interconnect substrate. Thereafter, the assembled chip array is inspected and tested.

Subsequent to being tested, the completed chip array is mounted to a package of the chip module. More particularly, the chip array is inserted into the cavity of the main body of the package such that the first interconnect pad array is in aligned contact with the second interconnect pad array provided on the interconnect shelf extending within the cavity of the main body. The first and second interconnect pad arrays are preferably attached to each other via soldering. In addition to the first and second interconnect pad arrays being soldered to each other, the interconnect substrate of the chip array may optionally be bonded to the main body of the package. After the chip array has been properly mounted to the main body of the package, the assembled chip array and main body are inspected and tested. Such inspection includes screening the assembly for proper burn-in, centrifuge, solderablility, etc.

Upon the completion of its testing, the assembled chip array and main body are preferably vacuum baked to remove moisture from the chip array (i.e., the interconnect substrate and packaged chips). Thereafter, the lid of the package is attached to the main body to enclose and seal the chip array within the package. The attachment of the lid to the main body may be accomplished through the use of a low temperature lid

seal or through the use of a low temperature welding process which creates a seam seal between the lid and the main body. Thereafter, the chip module is tested for fine and gross leaks of the enclosed cavity of the package, with the completed chip module then being given a final test.

BRIEF DESCRIPTION OF THE DRAWINGS

These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

Figure 1 is a top perspective view of a chip module constructed in accordance with the present invention with the lid of the package thereof being partially depicted;

Figure 2 is a cross-sectional view of the present chip module;

Figure 3 is a top view of the main body of the package of the present chip module;

Figure 4 is a cross-sectional view of the package of the present chip module, illustrating the lid of the package as being separated from the main body thereof;

Figure 5 is a top plan view of the interconnect substrate of the chip array of the present chip module;

Figure 6 is a bottom plan view of the interconnect substrate shown in Figure 5;

Figure 7A is a partial top plan view of the first interconnect pad array of the interconnect substrate shown in Figures 5 and 6;

Figure 7B is a partial cross-sectional view of the interconnect substrate shown in Figures 5 and 6, illustrating the manner in which vias extend between respective pairs of first and second sets of conductive interconnect pads of the first interconnect pad array;

Figure 8A is a top plan view of the assembled chip array of the present chip module;

Figure 8B is a side-elevational view of the chip array shown in Figure 8A; and

Figure 9 is a flow chart which describes the preferred sequence of steps used for assembling the present chip module.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawings wherein the showings are for purposes of illustrating a preferred embodiment of the present invention only, and not for purposes of limiting the same, Figure 1 perspectively illustrates a chip module 10 constructed in accordance with the present invention. As will be described in more detail below, the chip module 10 includes a universal package 12 for accommodating a selectively configurable chip array 14 (e.g., a memory array or logic array). Referring now to Figures 1, 2 and 5-8B, the chip array 14, which is a sub-assembly of the chip module 10, comprises an interconnect substrate 16 having opposed, generally planar surfaces, and in particular a top surface 18 and a bottom surface 20. In the preferred embodiment, the interconnect substrate 16 has a generally square configuration defining four peripheral edge segments. Disposed upon the top and bottom surfaces 18, 20 is a first interconnect pad array 22 of the interconnect substrate 16 which extends along one of the peripheral edge segments defined thereby. The first interconnect pad array 22 is used to facilitate the surface mounting of the chip array 14 to the package 12 in a manner which will be described in more detail below.

As best seen in Figures 5, 6, 7A and 7B, the first interconnect pad array 22 itself preferably comprises a first set of conductive interconnect pads 24 which are disposed on the top surface 18, and a second set of conductive interconnect pads 26 which are disposed on the

bottom surface 20. As indicated above, the conductive interconnect pads 24, 26 of the first and second sets, which collectively define the first interconnect pad array 22, extend along a common peripheral edge segment of the interconnect substrate 16. The conductive interconnect pads 24, 26 of the first and second sets are preferably though not necessarily arranged in identical patterns on the top and bottom surfaces 18, 20, respectively, such that the conductive interconnect pads 24 of the first set are aligned with respective ones of the conductive interconnect pads 26 of the second set. Additionally, a plurality of vias 28 are preferably extended through the interconnect substrate 16 between respective pairs of the conductive interconnect pads 24, 26 of the first and second sets for purposes of establishing electrical contact or communication between the pads 24, 26 of each pair. In the chip array 14, the first and second sets of conductive interconnect pads 24, 26 and associated vias 28 are formed through the use of conventional methodologies and are preferably fabricated from either gold or tin/lead. In this respect, the conductive interconnect pads 24, 26 are formed as conventional surface mount pads, with the vias 28 being conventionally formed as plated through-holes.

In addition to the first set of conductive interconnect pads 24 of the first interconnect pad array 22, disposed on the top surface 18 of the interconnect substrate 16 is a first set of conductive lead pads 30. Similarly, disposed on the bottom surface 20 of the interconnect substrate 16 is a second set of conductive lead pads 32. In the chip array 14, the interconnect substrate 16 is formed such that the conductive lead pads 30, 32 of the first and second sets are electrically connected to the first interconnect pad array 22. In this respect, though not shown, those of ordinary skill in the art will recognize that the conductive lead pads 30, 32 of the first and second sets and conductive

interconnect pads 24, 26 of the first interconnect pad array 22 are electrically interconnected by conventional traces which form a printed circuit upon the interconnect substrate 16.

In addition to the interconnect substrate 16, the chip array 14 of the chip module 10 comprises a plurality of packaged chips 34, each of which comprises a body 36 having a plurality of chip pins or leads 38 protruding from respective ones of the opposed lateral edges thereof. As indicated above, the chip array 14 may comprise a memory array or a logic array, with each of the packaged chips 34 therefore preferably being either a memory device or a logic device. Although by way of example and not limitation, the packaged chips 34 may comprise conventional chip packages, such as a TSOP I package, a TSOP II package, a QFP package, and/or a CSP package. However, other packaged chips are expressly contemplated herein. In the chip array 14, the chip leads 38 of two packaged chips 34 are electrically connected to respective ones of the conductive lead pads 30 of the first set disposed upon the top surface 18, with the chip leads 38 of two packaged chips 34 being electrically connected to respective ones of the conductive lead pads 32 of the second set disposed upon the bottom surface 20.

The attachment of the chip leads 38 of the packaged chips 34 to the conductive lead pads 30, 32 of the first and second sets is preferably accomplished via soldering in accordance with conventional methodologies. As such, the chip array 14 includes a total of four packaged chips 34. However, those of ordinary skill in the art will recognize that the chip array 14 may be provided with fewer or greater than four packaged chips 34, and that the conductive lead pads 30, 32 may be provided on only the top surface 18 or the bottom surface 20 of the interconnect substrate 16. Additionally, it is contemplated that one or more non-packaged integrated

circuit chips may be attached to the interconnect substrate 16 and electrically connected to the first interconnect pad array 22 as an alternative to the integrated circuit chip being incorporated into a packaged chip 34. Like the conductive interconnect pads 22, 24 of the first and second sets, the conductive lead pads 30, 32 of the first and second sets are preferably fabricated from either gold or tin/lead.

Though the interconnect substrate 16 of the chip array 14 may be of a rigid construction, the same is preferably flexible and formed to have a thickness not exceeding about 0.015 inches. As indicated above, this minimal thickness of the interconnect substrate 16, which results in its flexibility, provides the assembled chip array 14 with a thin profile. The interconnect substrate 16 is preferably fabricated from a polyamide, though alternative materials possessing similar characteristics may also be employed in relation thereto. Additionally, as best seen in Figures 5 and 6, the interconnect substrate 16 is preferably formed to include a pair of notches 40 disposed within respective ones of the peripheral edge segments thereof which extend in generally perpendicular relation to the peripheral edge segment along which the first and second sets of conductive interconnect pads 24, 26 of the first interconnect pad array 22 are extended. The use of the notches 40 will be described in more detail below.

Referring now to Figures 1-4, the package 12 of the chip module 10 comprises a generally square main body 42 and a lid 44 which is attachable to the main body 42 in a manner which will also be described in more detail below. The main body 42 itself defines a cavity 46 which is sized and configured to receive the chip array 14. Extending within and along one side of the cavity 46 is a generally planar interconnect shelf 48 which includes a second interconnect pad array 50 disposed thereon. The second interconnect pad array 50 comprises a third set of

conductive interconnect pads 52 which are arranged upon the interconnect shelf 48 in a pattern identical to those of the first and second sets of conductive interconnect pads 24, 26 of the chip array 14. In the chip module 10, a total of seventy-one conductive interconnect pads 24, 26, 52 are included in each of the first, second and third sets thereof. Like the conductive interconnect pads 24, 26 of the first and second sets, the conductive interconnect pads 52 of the third set are also preferably fabricated from either gold or tin/lead.

As best seen in Figures 1, 3 and 4, the main body 42 of the package 12 includes a plurality of package leads 54 which protrude therefrom and have inwardly turned or curved distal ends. In the chip module 10, the main body 42 of the package 12 is formed such that the package leads 54 are electrically connected to the second interconnect pad array 50. The main body 42 preferably includes sixty-eight package leads 54 which extend about the periphery thereof. More particularly, the package leads 54 collectively define JEDEC sixty-eight pin JLCC mechanical and industry standard pinouts. However, those of ordinary skill in the art will further recognize that the main body 42 may be provided with differing numbers of package leads 54 extending therefrom to define other standard pin configurations depending on the desired use of the chip module 10. The package 12 (i.e., the main body 42 and lid 44) is preferably fabricated from co-fired alumina, though alternative materials possessing similar characteristics may also be employed in relation thereto.

In the chip module 10 of the present invention, the chip array 14 is insertable into the cavity 46 of the main body 42 such that the first and second interconnect pad arrays 22, 50 are in aligned contact with each other. Due to the conductive interconnect pads 24, 26, 52 of the first, second and third sets being provided in identical patterns, the proper insertion of the chip array 14 into

the cavity 46 of the main body 42 will result in the conductive interconnect pads 24, 26 of either the first or second sets being in aligned (i.e., registered) contact with respective ones of the conductive interconnect pads 52 of the third set. It is contemplated that the chip array 14 may be inserted into the cavity 46 such that either the conductive interconnect pads 24 of the first set or the conductive interconnect pads 26 of the second set are in aligned contact with the conductive interconnect pads 52 of the third set. Subsequent to the insertion of the chip array 14 into the cavity 46 and the electrical connection of the first and second interconnect pad arrays 22, 50 to each other in a prescribed manner, the attachment of the lid 44 to the main body 42 encloses and seals the chip array 14 within the package 12.

As best seen in Figure 3, the main body 42 of the package 12 is preferably formed to include an opposed pair of tabs 56 which extend along opposed end portions of the interconnect shelf 48 and are insertable into respective ones of the notches 40 of the interconnect substrate 16 when the chip array 14 is inserted into the cavity 46. Advantageously, the receipt of the tabs 56 into the registry notches 40 facilitates a proper registry between the first and second interconnect pad arrays 22, 50. As seen in Figures 3, 5, 6 and 8A, the notches 40 are preferably formed to be of differing sizes, with the tabs 56 also being of differing sizes which are receivable into respective ones of the notches 40. This sizing difference allows the chip array 14 to be inserted into the cavity 46 in only one prescribed orientation. As such, though the conductive interconnect pads 22, 24 of either the first or second sets may be placed into direct contact with the conductive interconnect pads 52 of the third set, the chip array 14 must be appropriately configured such that the desired

electrical connections are achieved when the tabs 56 are inserted into the notches 40.

Having thus described the structural attributes of the chip module 10, the preferred method of assembling the same will now be described with particular reference to Figure 9. The preferred method comprises the initial step of assembly the chip array 14 of the chip module 10 in the previously described manner. As indicated above, such assembly is preferably accomplished by attaching one or more packaged chips 34 to one or both of the top and bottom surfaces 18, 20 of the interconnect substrate 16 through the use of conventional surface mount assembly techniques such that the packaged chip(s) 34 are mounted and electrically connected to respective ones of either the first and/or second sets of conductive lead pads 30, 32, and hence the first interconnect pad array 22 of the interconnect substrate 16. Thereafter, the assembled chip array 14 may be inspected and tested to ensure proper function and electrical contact between the packaged chip(s) 34 and the interconnect substrate 16.

Subsequent to being tested, the assembled chip array 14 is mounted to the main body 42 of the package 12. More particularly, the chip array 14 is inserted into the cavity 46 of the main body 42 such that the tabs 56 are received into respective ones of the notches 40, thus facilitating the proper registry and aligned contact between the first and second interconnect pad arrays 22, 50. The first and second interconnect pad arrays 22, 50 are preferably electrically connected to each other via conventional soldering techniques. In addition to the first and second interconnect pad arrays 22, 50 being soldered to each other, the interconnect substrate 16 of the chip array 14 may optionally be bonded to the main body 42 of the package 12. After the chip array 14 has been properly mounted to the main body 42, the assembled chip array 14 and main body 42 may be inspected and

tested. Such inspection includes screening the assembly for proper burn-in, centrifuge, solderability, etc.

Upon the completion of its testing, the assembled chip array 14 and main body 42 are preferably vacuum baked to remove moisture from the chip array 14 (i.e., the interconnect substrate 16 and packaged chip(s) 34). Thereafter, the lid 44 of the package 12 is attached to the main body 42 to enclose and seal the chip array 14 within the package 12. The attachment of the lid 44 to the main body 42 may be accomplished through the use of a low temperature lid seal or seal ring 58 which is preferably fabricated from covar. Alternatively, the attachment of the lid 44 to the main body 42 may be accomplished through the use of a low temperature welding process which creates a seam seal between the lid 44 and main body 42. Subsequent to the attachment of the lid 44 to the main body 42, the chip module 10 is tested for fine and gross leaks of the enclosed cavity 46 of the package 12, with the completed chip module 10 then being given a final test.

As indicated above, the package 12 of the present chip module 10 is universal in that the same is capable of accommodating any one of differently configured chip arrays 14 which include the interconnect substrate 16. As such, a modification to the functional attributes of the chip module 10 requires only a change in the printed circuit on the interconnect substrate 16 to accommodate differing memory and/or logic devices, with no change being required for the package 12. The relative ease and low cost of making changes to the printed circuit on the interconnect substrate 16, coupled with the lack of a need for changes in the tooling used to fabricate the package 12, permits rapid upgrades or changes in the chip module 10 to avoid obsolescence.

Additional modifications and improvements of the present invention may also be apparent to those of ordinary skill in the art. For example, the chip array

14 of the chip module 10 may comprise a chip stack mounted to the interconnect substrate 16, with the cavity 46 of the main body 42 and lid 44 being configured to accommodate such chip array 14. Thus, the particular combination of parts and steps described and illustrated herein is intended to represent only one embodiment of the present invention, and is not intended to serve as limitations of alternative devices within the spirit and scope of the invention.

CLAIMS:

1. A chip module, comprising:

a chip array comprising:

an interconnect substrate having opposed, generally planar surfaces and including a first interconnect pad array disposed on at least one of the surfaces thereof; and

at least one integrated circuit chip attached to the interconnect substrate and electrically connected to the first interconnect pad array;

a package comprising:

a main body defining a cavity sized and configured to receive the chip array and having a generally planar interconnect shelf which extends within the cavity and includes a second interconnect pad array disposed thereon; and

a lid attachable to the main body in a manner enclosing and sealing the cavity;

the chip array being insertable into the cavity such that the first and second interconnect pad arrays are in aligned contact with each other and the attachment of the lid to the main body encloses and seals the chip array within the package.

2. The chip module of Claim 1 wherein the interconnect substrate of the chip array has a generally square configuration defining four peripheral edge segments, and the first interconnect pad array extends along one of the peripheral edge segments.

3. The chip module of Claim 2 wherein the first interconnect pad array comprises:

first and second sets of conductive interconnect pads disposed on respective ones of the opposed surfaces of the interconnect substrate and extending along a common peripheral edge segment thereof, the conductive interconnect pads of the

first and second sets being arranged in identical patterns such that the conductive interconnect pads of the first set are aligned with respective ones of the conductive interconnect pads of the second set; and

a plurality of vias extending through the interconnect substrate between respective pairs of the conductive interconnect pads of the first and second sets.

4. The chip module of Claim 3 wherein the second interconnect pad array comprises a third set of conductive interconnect pads which are arranged upon the shelf in a pattern identical to those of the first and second sets of conductive interconnect pads.

5. The chip module of Claim 4 wherein seventy-one conductive interconnect pads are included in each of the first, second and third sets thereof.

6. The chip module of Claim 1 wherein the main body of the package includes a plurality of package leads which protrude therefrom and are electrically connected to the second interconnect pad array.

7. The chip module of Claim 6 wherein the main body includes sixty-eight package leads.

8. The chip module of Claim 1 wherein the interconnect substrate of the chip array is flexible.

9. The chip module of Claim 8 wherein the interconnect substrate is formed to have a thickness not exceeding about 0.015 inches.

10. The chip module of Claim 8 wherein the interconnect substrate is fabricated from a polyamide.

11. The chip module of Claim 1 wherein the package is fabricated from co-fired alumina.

12. The chip module of Claim 2 wherein:

the interconnect substrate of the chip array includes a pair of notches disposed within respective ones of the peripheral edge segments thereof which extend in generally perpendicular

relation to the peripheral edge segment along which the first interconnect pad array is extended; and

the main body of the package is formed to include an opposed pair of tabs which are insertable into respective ones of the notches when the chip array is inserted into the cavity;

the receipt of the tabs into the notches facilitating a proper registry between the first and second interconnect pad arrays.

13. The chip module of Claim 1 wherein:

the interconnect substrate of the chip array includes a plurality of conductive lead pads which are disposed on at least one of the opposed surfaces thereof and are electrically connected to the first interconnected pad array; and

the integrated circuit chip is incorporated into a packaged chip having a plurality of chip leads protruding therefrom which are electrically connected to respective ones of the conductive lead pads.

14. The chip module of Claim 13 wherein the interconnect substrate includes a plurality of conductive lead pads disposed on respective ones of the opposed surfaces thereof and the chip leads of at least two packaged chips are electrically connected to the conductive lead pads on respective ones of the opposed surfaces of the interconnect substrate.

15. The chip module of Claim 14 wherein the chip array comprises a memory array and each of the packaged chips is a memory device selected from the group consisting of:

a TSOP I package;

a TSOP II package;

a QFP package; and

a CSP package.

16. The chip module of Claim 14 wherein the chip array is a logic array and each of the packaged chips is a logic device selected from the group consisting of:

a TSOP I package;

a TSOP II package;

a QFP package; and

a CSP package.

17. A chip module, comprising:

a chip array comprising:

an interconnect substrate having opposed, generally planar surfaces and including a first interconnect pad array disposed on at least one of the surfaces thereof; and

at least one packaged chip attached to the interconnect substrate and electrically connected to the first interconnect pad array;

a package defining an interior cavity having a generally planar interconnect shelf which extends therewithin and includes a second interconnect pad array disposed thereon;

the chip array being insertable into the cavity such that the first and second interconnect pad arrays are in aligned contact with each other.

18. A method of assembling a chip module, comprising the steps of:

(a) assembling a chip array of the chip module;

(b) testing the chip array;

(c) mounting the chip array to a package of the chip module;

(d) testing the assembled chip array and package;

(e) enclosing and sealing the chip array within the package; and

(f) testing the completed chip module.

19. The method of Claim 18 wherein step (a) comprises the steps of:

(1) providing an interconnect substrate having opposed, generally planar surfaces and including a first interconnect pad array disposed on at least one of the surfaces thereof; and

(2) attaching at least one integrated circuit chip to the interconnect substrate such that the integrated circuit chip is electrically connected to the first interconnect pad array.

20. The method of Claim 19 wherein step (2) comprises attaching at least two packaged chips to respective ones of the opposed surfaces of the interconnect substrate.

21. The method of Claim 18 wherein step (b) comprises inspecting the assembled chip array prior to the testing thereof.

22. The method of Claim 19 wherein step (c) comprises the steps of:

(1) providing a main body defining a cavity sized and configured to receive the chip array and having a generally planar interconnect shelf which extends within the cavity includes a second interconnect pad array disposed thereon;

(2) inserting the chip array into the cavity such that the first interconnect pad array is in aligned contact with the second interconnect pad array; and

(3) soldering the first and second interconnect pad arrays to each other.

23. The method of Claim 22 wherein step (3) further comprises bonding the interconnect substrate of the chip array to the main body of the package.

24. The method of Claim 22 wherein step (d) comprises inspecting the assembled chip array and main body prior to the testing thereof.

25. The method of Claim 22 wherein step (e) comprises attaching a lid of the package to the main body to enclose and seal the chip array within the package.

26. The method of Claim 25 wherein step (e) comprises vacuum baking the assembled chip array and main body to remove moisture from the chip array prior to attaching the lid to the main body.

27. The method of Claim 25 wherein step (e) comprises attaching the lid to the main body through the use of a low temperature lid seal.

28. The method of Claim 25 wherein step (e) comprises attaching the lid to the main body through the use of a low temperature welding process.

29. The method of Claim 25 wherein step (f) comprises testing for fine and gross leaks of the enclosed cavity of the package.

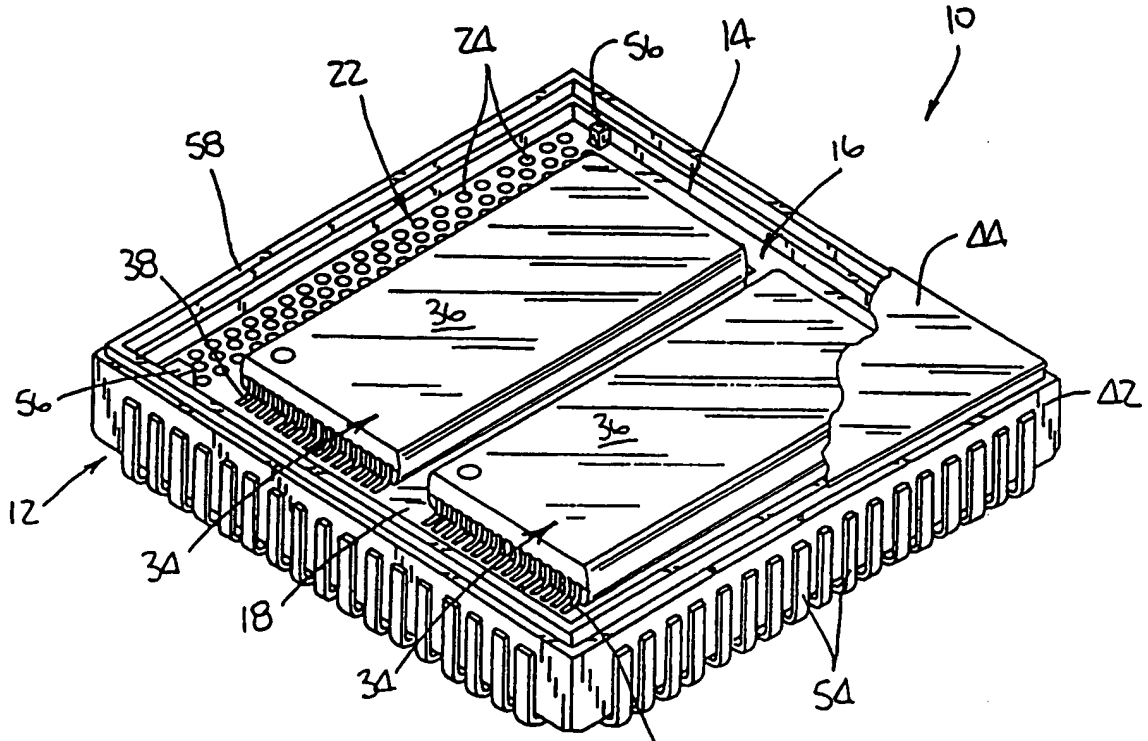
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Fig. 1

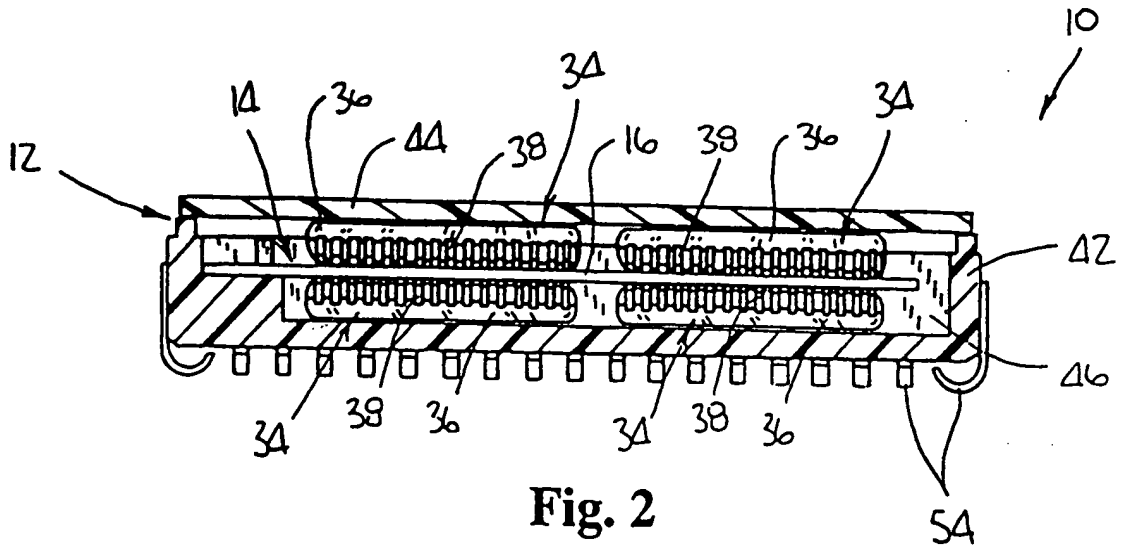
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Fig. 2

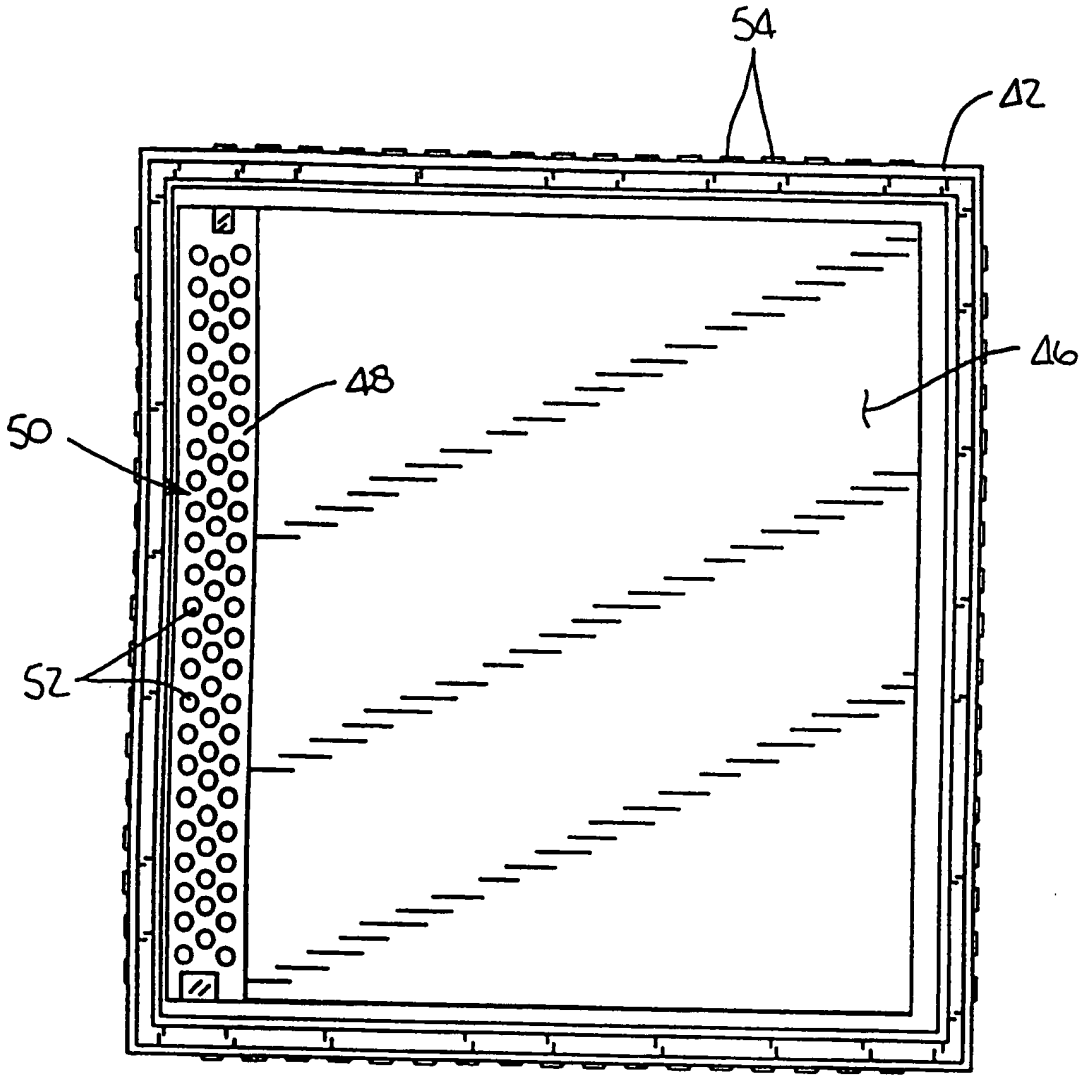

Fig. 3

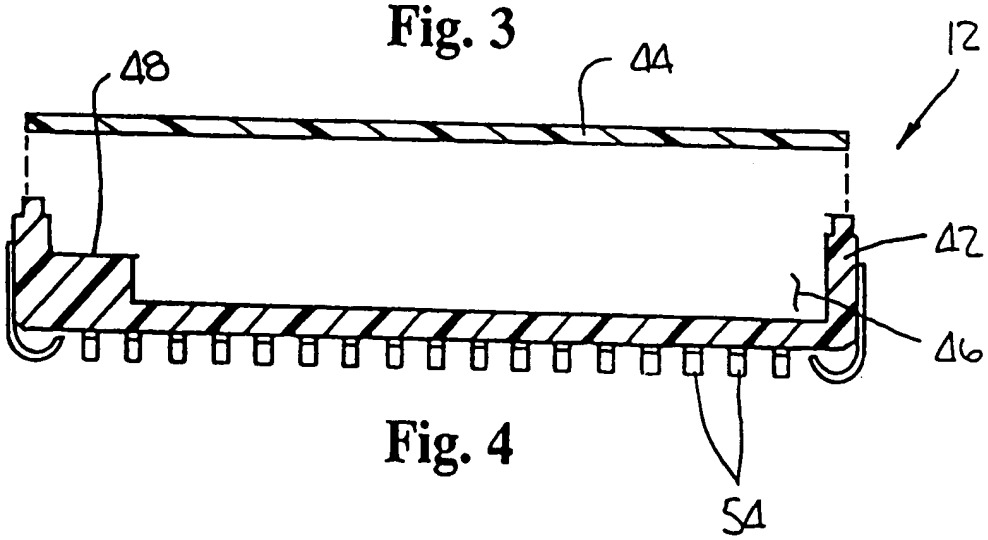

Fig. 4

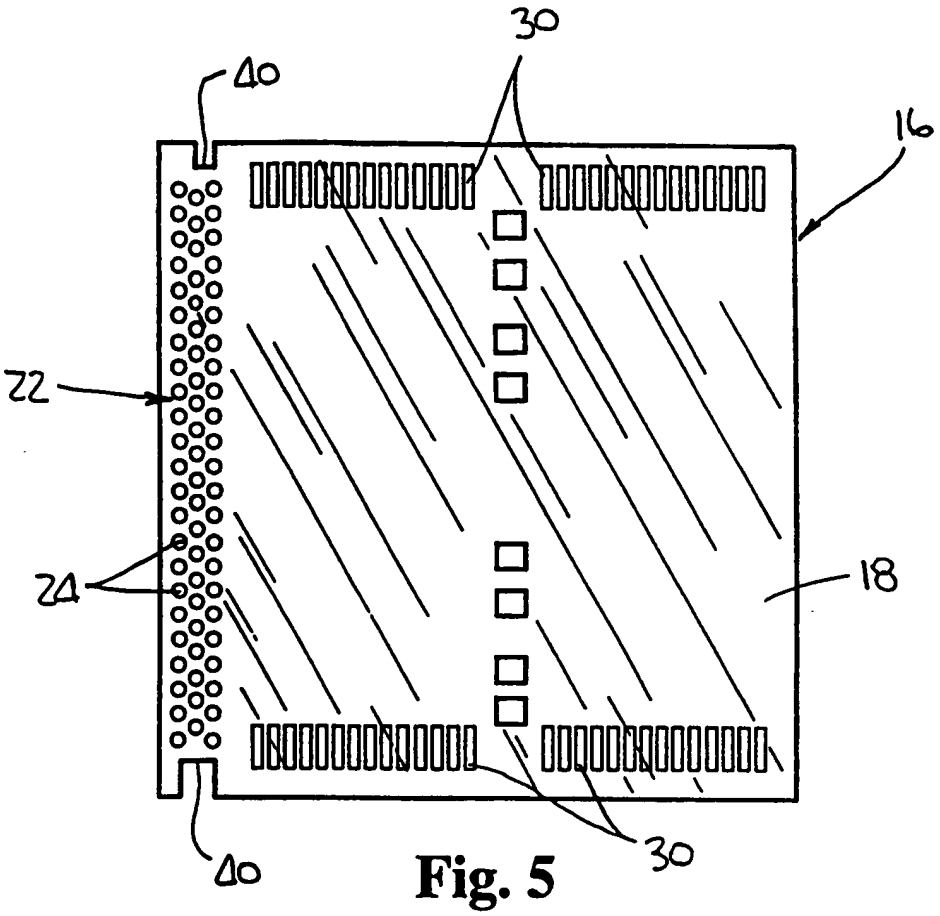

Fig. 5

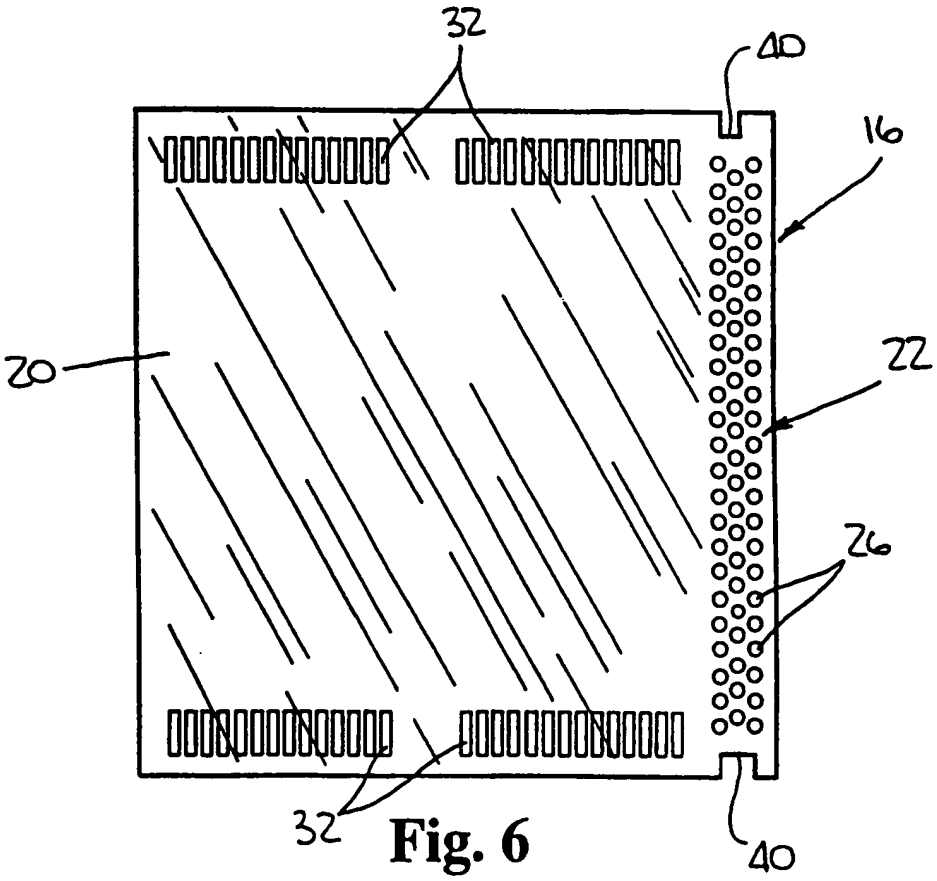

Fig. 6

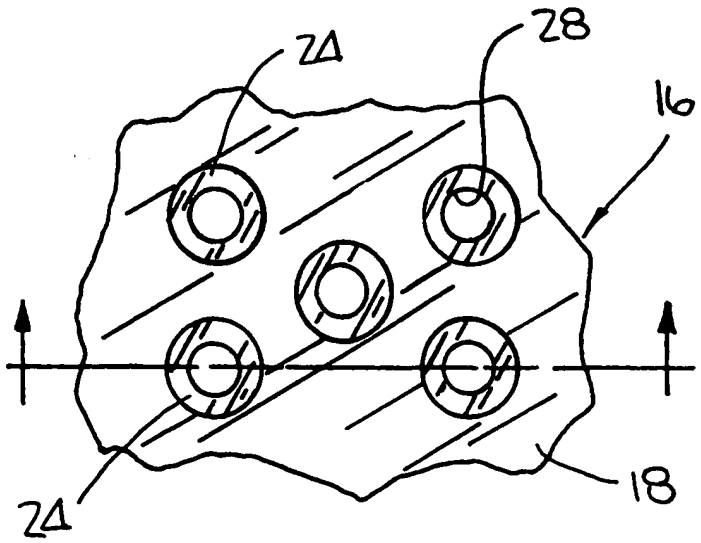

Fig. 7A

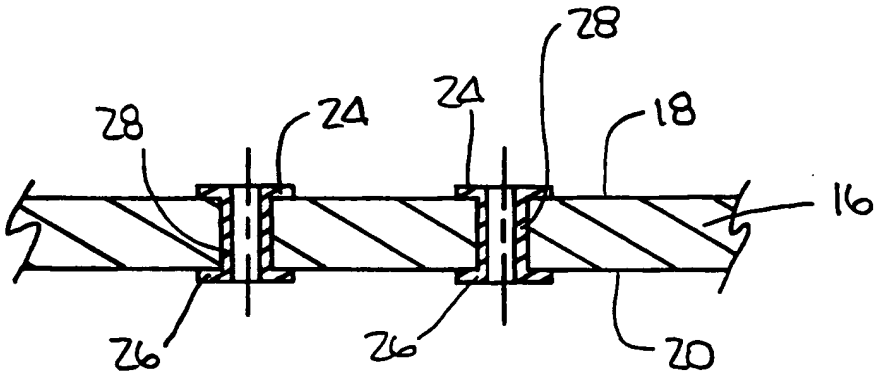

Fig. 7B

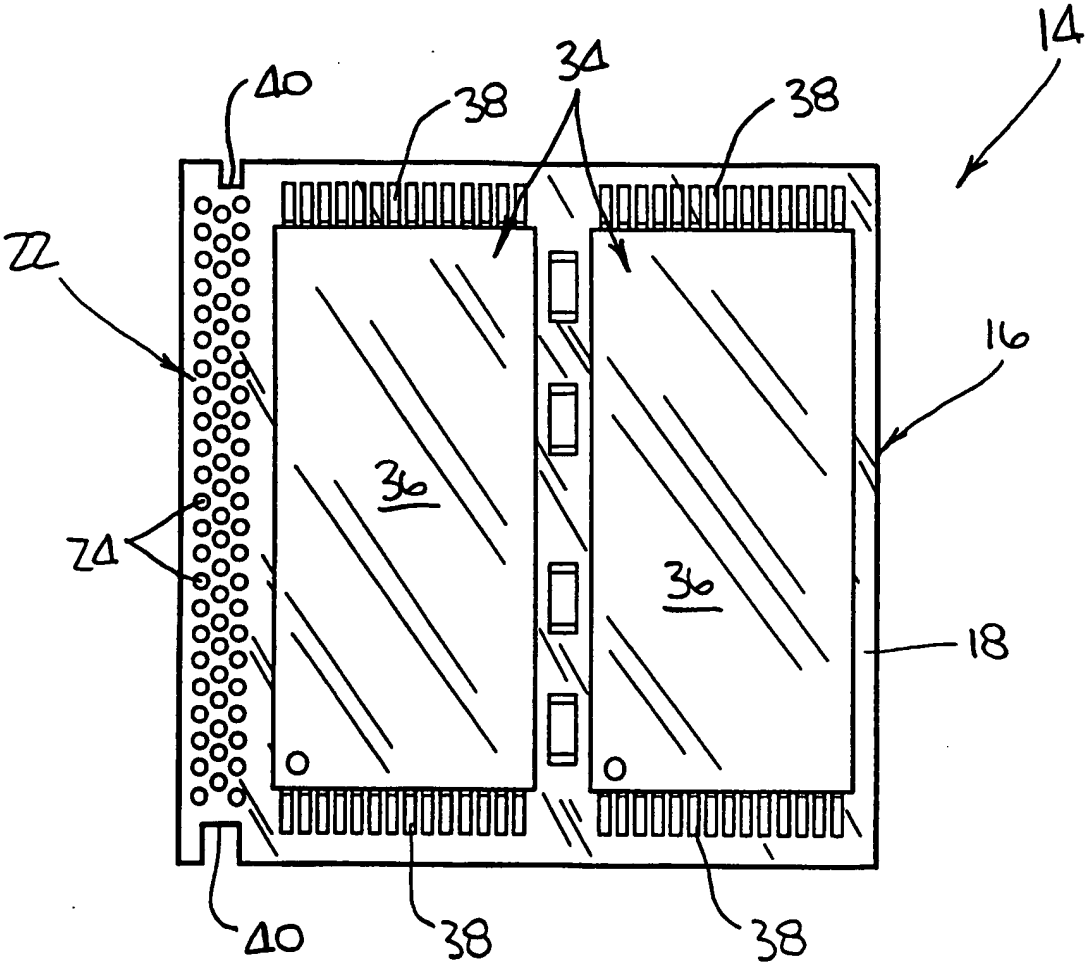
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Fig. 8A

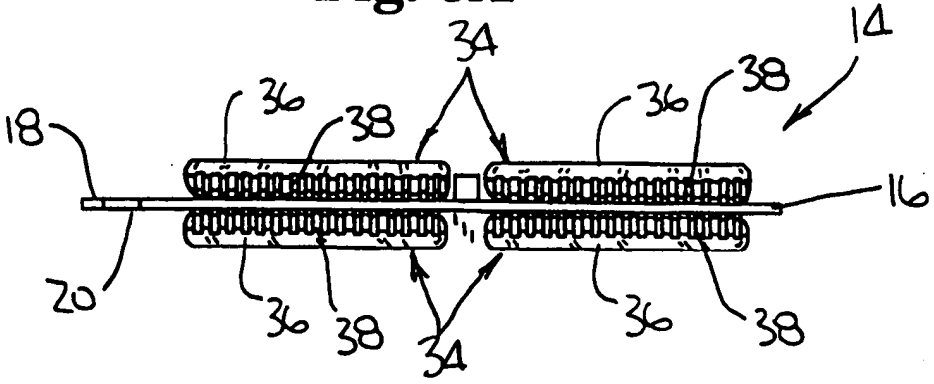
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Fig. 8B

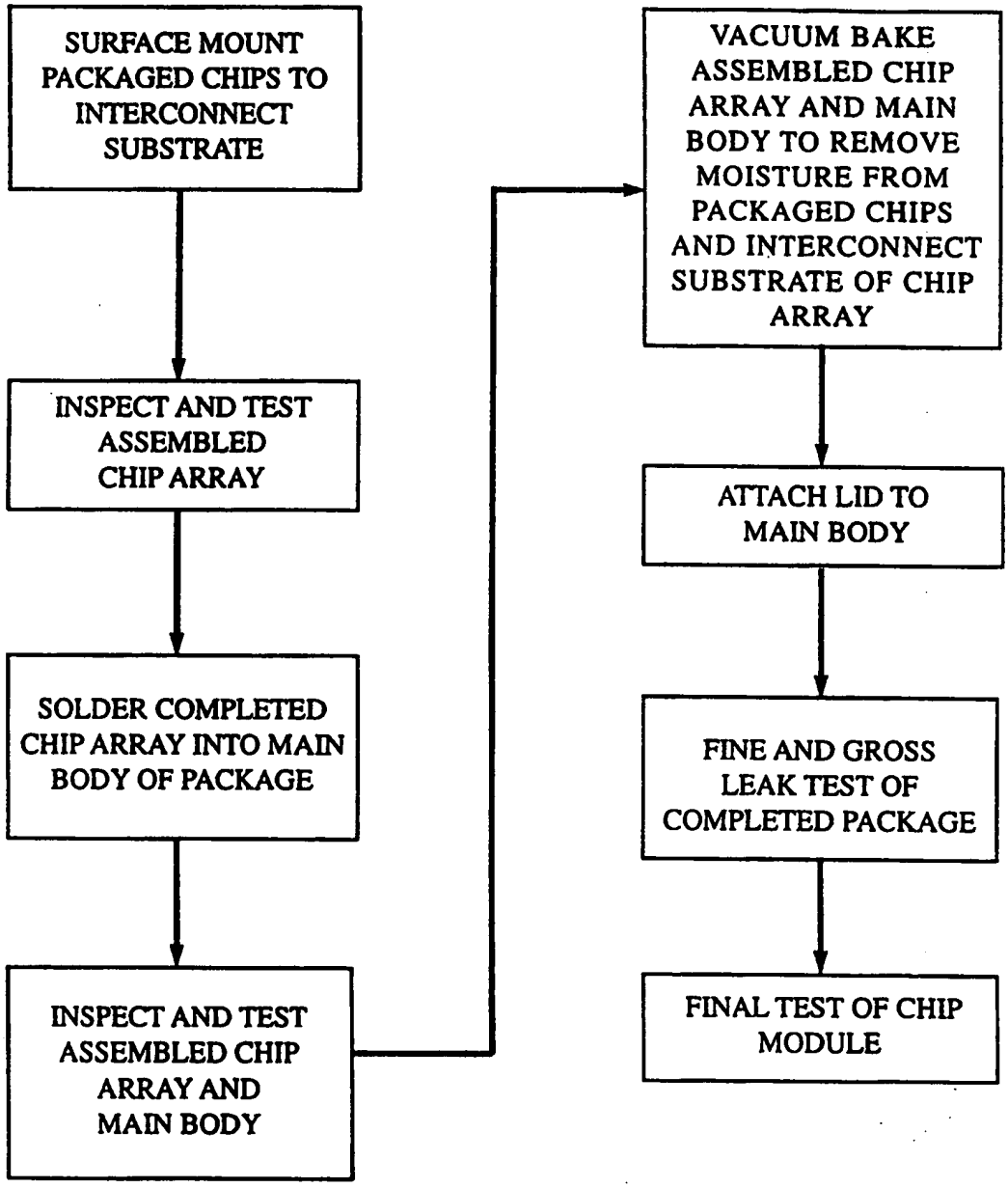
SURFACE MOUNT PACKAGED CHIPS TO INTERCONNECT SUBSTRATE
INSPECT AND TEST ASSEMBLED CHIP ARRAY
SOLDER COMPLETED CHIP ARRAY INTO MAIN BODY OF PACKAGE
INSPECT AND TEST ASSEMBLED CHIP ARRAY AND MAIN BODY
VACUUM BAKE ASSEMBLED CHIP ARRAY AND MAIN BODY TO REMOVE MOISTURE FROM PACKAGED CHIPS AND INTERCONNECT SUBSTRATE OF CHIP ARRAY
ATTACH LID TO MAIN BODY
FINE AND GROSS LEAK TEST OF COMPLETED PACKAGE
FINAL TEST OF CHIP MODULE

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/04988

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 23/02, 23/043, 23/10, 23/15
US CL :257/704, 723; 361/764; 438/15
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/679, 704, 723, 777; 361/761, 764, 767; 438/14, 15, 125

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO APS EAST
search terms: cap, lid, cavity, recess

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y --- A	US 5,731,633 A (CLAYTON) 24 March 1998 (24-03-1998), Figs. 1 and 2; col.5, lines 31-35; col.8, lines 47-52 and 58-62; col.9, lines 5-13.	1-2, 8-9 ------ 10 ------ 12-16, 19-20, 22-29
X --- Y	US 5,869,896 A (BAKER et al.) 09 February 1999 (09-02-1999), Figs. 5 and 7-9; col.5, line 22; col.6, lines 18-26 and 37-43; col.9, lines 7-11.	1-8 ------ 10, 11
Y	US 5,818,106 A (KUNIMATSU) 06 October 1998 (06-10-1998), Fig. 1.	11

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance	
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"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	
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Date of the actual completion of the international search 28 APRIL 2000	Date of mailing of the international search report 22 MAY 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JOHN B. VIGUSHIN Telephone No. (703) 308-0956

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/04988

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,712,767 A (KOIZUMI) 27 January 1998 (27-01-1998), Figs. 4A, 4B, 4C and 5; col. 3, lines 52-55 and 63-64; col. 4, lines 16-21.	17
X	US 4,285,002 A (CAMPBELL) 18 August 1981 (18-08-1981), Figs. 1 and 7.	18, 21